Sem III CBGS (Electronics) 09/12/1

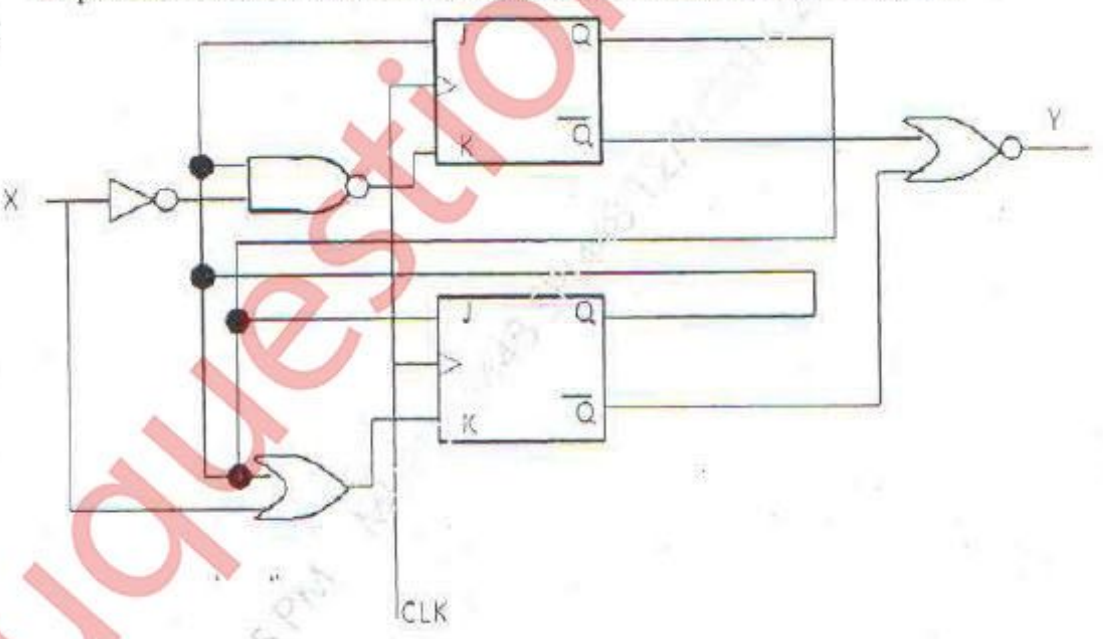
Digital Circuit & Design

QP Code :547501

(3 hours) **Total Marks :80**

N.B.:

1. Question No. 1 is **compulsory.**
2. Attempt any **3Questions** from the remaining 5 Questions
3. **Assume suitable data, wherever necessary**

Q. No	Solve any four	Marks
Q 1.(a)	Write a truth table of half adder and write a VHDL code for half adder	5
Q 1.(b)	Explain advantages of JTAG architecture	5
Q 1.(c)	Explain advantages and drawback of synchronous counter.	5
Q 1.(d)	Explain the following terms: 1.Noise margin 2. Noise immunity 3. Propagation delay with reference to digital ICs	5
Q 1.(e)	Differentiate between multiplexer and demultiplexer	5
Q2.(a)	Design a Meal type sequence detector to detect three or more consecutive 1's in a string of bits coming through an input line.	10
Q 2.(b)	What are universal gates? Why are they called so? Implement XOR and XNOR function using all NAND gates.	10
Q 3.(a)	 Analyze the sequential state machine shown in figure and obtain state diagram for the same	10
Q 3.(b)	Obtain excitation table for JK flip flop and convert JK flip flop to T flip flop.	10
Q 4.(a)	Draw a circuit diagram of 2 input TTL NAND gate and Explain the interfacing of TTL and CMOS.	10

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Q4.(b)	Design a MOD10 asynchronous counter using T flip flop	10
Q5(a)	Design a combinational circuit using a suitable PAL considering the following Boolean expressions. Use a PAL with four inputs and four outputs and three wide AND OR structure. $W(a,b,c,d)= \sum m(2,12,13)$ $X(a,b,c,d)=\sum m(7,8,9,10,11,12,13.14,15)$	10
Q5(b)	Design 4 bit Johnson counter using J-K flip flop. Explain its working using waveform	10
Q6(a)	Write short notes on 1. Stuck at zero and stuck at 1fault. 2. Entity declaration and architecture declaration. 3. FPGA architecture 4. State reduction and state assignment.	20